Abstract of the Disclosure:

A method for manufacturing a chip housing includes a first basis having a photolithograpically structurable layer on a main face, structured into a cover. A chip has the structur at a main face between first contact elements. A second photolithograpically structurable layer applied to the main face is structured forming a recess surrounded by a wall ne the structure exposing the first contact elements. Then, th first basis and the chip are merged with the structure and the cover facing and aligned with each other, and the reces closed by the cover. Removing the first basis leads to an o chip cavity. Afterwards, a second basis and the chip are merged with the first contact elements connected to the second basis via a conductive structure. Afterwards, the second basis is removed for exposing the conductive structure. The method is less subject to cost and size limitations of known housing technologies.